With regard to the rejection of claims 1-3, 5, 6, 9-11, 13, 14, 17-19, 21 and 22 under 35 U.S.C. §103(a) as being unpatentable over Itri, Applicant asserts that such claims recite elements of the present invention that are not described or suggested by Itri.

Itri discloses a timing recovery system, which enables two or more receivers at one end of a digital subscriber loop to share a single analog-to-digital converter, while still allowing optimal phasing of each receiver clock relative to its received signal. The respective receiver clocks are phase offset by a fixed amount.

Independent claims 1, 9 and 17 recite that a digital subscriber line transport signal includes frequency and phase information associated with a transmitter-side timing reference signal. Additionally, a local oscillator is provided in the transmitter and adapted to receive the transmitter-side timing reference signal as an external timing reference. Furthermore, upon receiving the transport signal at the receiver, the frequency and phase information is recovered and a receiver-side timing reference signal is derived and used to control timing in the receiver.

The Examiner contends that Itri discloses a master timing source supplied by the central office and a remote terminal that derives the timing information from the received signal. However, even if these assertions are assumed to be correct, Itri fails to disclose, and the Examiner fails to address, the limitations relating to the processing in the transmitter of a payload signal and a transmitter-side timing reference signal to generate a digital subscriber line transport signal including frequency and phase information associated with the transmitter-side timing reference signal, as expressly recited in independent claims 1, 9 and 17.

The Examiner also contends that the phase adjust and phase error detect blocks shown in FIG. 5 of Itri represent a local oscillator. However, it is unclear whether the Examiner contends that one, both or a combination of the phase adjust and phase error detect blocks represent the local oscillator. More specifically, phase adjust block 218 adjusts the phase of the master clock based on a phase error detected in order to produce a new transmit clock signal. Therefore, Itri does not disclose a local oscillator adapted to configure the digital subscriber line transport signal to include the frequency and phase information associated with the transmitter-side timing reference signal.

Even if the Examiner's assertions regarding the phase adjust and phase error detect blocks are assumed to be correct, the Examiner acknowledges that Itri fails to teach that the phase adjust and phase error detect blocks are part of the transmitter. The Examiner then contends that all of the

components on the left side of FIG. 5, representing the central office station, can be grouped together as the transmitter. While it is true that signals are transmitted from the central office station, there are two specific elements in the central office station labeled as transceivers. Thus, the entire central office station cannot be considered a transmitter when two specific components that exist within it are labeled as transceivers and perform separate transmitting functions.

Further, while the Examiner contends that block diagrams may represent separate functions and do not necessarily represent separate components, Itri specifically states in column 5, lines 12-14, that "FIG. 5 illustrates the primary components of the clock recovery phase control circuits." Thus, the transceiver and phase blocks in FIG. 5 represent separate components. Therefore, Itri fails to disclose a local oscillator provided in the transmitter and adapted to receive the transmitter-side timing reference signal as an external timing reference, as expressly recited in independent claims 1, 9 and 17.

Applicant asserts that dependent claims 2, 3, 5, 6, 10, 11, 13, 14, 18, 19, 21 and 22 are patentable for at least the reasons identified above with regard to independent claims 1, 9 and 17. Applicant further asserts that dependent claims 2, 3, 5, 6, 10, 11, 13, 14, 18, 19, 21 and 22 contain patentable subject matter in their own right. Accordingly, withdrawal of the §103(a) rejection of claims 1-3, 5, 6, 9-11, 13, 14, 17-19, 21 and 22 is respectfully requested.

With regard to the rejection of claims 4, 12 and 20 under 35 U.S.C. §103(a) as being unpatentable over Itri in view of Near, Applicant asserts that such claims are patentable for at least the reasons that their respective independent claims are patentable.

A proper *prima facie* case of obviousness requires that the cited references, when combined, must "teach or suggest all the claim limitations." See M.P.E.P., Eighth Edition, August 2001, §706.02(j). Applicant submits that the Examiner has failed to establish a proper *prima facie* case of obviousness in the present §103(a) rejection, in that the Itri and Near references, even if assumed to be combinable, fail to teach or suggest all the claim limitations.

The Examiner, in formulating the §103(a) rejection, acknowledges that the Itri reference fails to teach or suggest using stratum 1 traceable synchronization information. See the Office Action at page 3, paragraph 4. However, the Examiner nonetheless argues that the claimed arrangements

would be obvious in view of the combined teachings of Itri and Near. Applicant respectfully disagrees.

The Examiner characterizes the Near reference as teaching "a method for synchronizing interconnected digital equipment and further teaches the basic concept of the stratum level" (Office Action, page 3, paragraph 4 through page 4, paragraph 1). Even if one were to assume that this characterization of Near is correct, the combined teachings of Itri and Near still fail to meet the above-cited claim limitations. The combination of Itri and Near fails to disclose the elements of independent claims 1, 9 and 17 distinguished above. Further, the combination fails to disclose stratum 1 traceable synchronization information in a timing reference signal received by the local oscillator in the transmitter.

From the foregoing, it is apparent that each of claims 4, 12 and 20 includes at least one limitation which is not taught or suggested by the proposed combination of Itri and Near. The combined teachings of these references therefore fail to "teach or suggest all the claim limitations" as would be required by a proper §103(a) rejection. Therefore, the proposed combination of Itri and Near fails to establish a *prima facie* case of obviousness under 35 U.S.C. §103(a). Accordingly, withdrawal of the §103(a) rejection of claims 4, 12 and 20 is respectfully requested.

With regard to the rejection of claims 7, 8, 15 and 16 under 35 U.S.C. §103(a) as being unpatentable over Itri in view of Narasimha, Applicant asserts that such claims are patentable for at least the reasons that their respective independent claims are patentable.

Applicant submits that the Examiner has failed to establish a proper *prima facie* case of obviousness in the present §103(a) rejection, in that the Itri and Narasimha references, even if assumed to be combinable, fail to teach or suggest all the claim limitations.

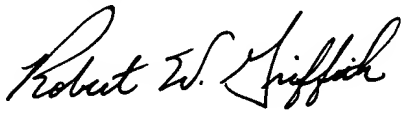
The Examiner, in formulating the §103(a) rejection, acknowledges that the Itri reference fails to teach or suggest a timing reference signal generated by a building integrated timing supply having GPS capability, as well as a transmitted clock generated by an add-drop multiplexer associated with the transmitter. See the Office Action at page 4, paragraph 2. However, the Examiner nonetheless argues that the claimed arrangements would be obvious in view of the combined teachings of Itri and Narasimha. Applicant respectfully disagrees.

The Examiner characterizes the Narasimha reference as teaching that "in a digital network, there is a plurality of primary reference source checks implemented using GPS receiver technology" (Office Action, page 4, paragraph 2). Even if one were to assume that this characterization of Narasimha is correct, the combined teachings of Itri and Narasimha still fail to meet the above-cited claim limitations. The combination of Itri and Narasimha fails to disclose the elements of independent claims 1, 9 and 17 distinguished above. Further, the combination fails to disclose a timing reference signal, received by the local oscillator in the transmitter, that is generated by a building integrated timing supply having GPS capability. The combination also fails to disclose a timing reference signal, received by the local oscillator in the transmitter, having a transmit clock generated by an add-drop multiplexer associated with the transmitter.

From the foregoing, it is apparent that each of claims 7, 8, 15 and 16 includes at least one limitation which is not taught or suggested by the proposed combination of Itri and Narasimha. The combined teachings of these references therefore fail to "teach or suggest all the claim limitations" as would be required by a proper §103(a) rejection. Therefore, the proposed combination of Itri and Narasimha fails to establish a *prima facie* case of obviousness under 35 U.S.C. §103(a). Accordingly, withdrawal of the rejection of claims 7, 8, 15 and 16 under §103(a) is respectfully requested.

In view of the above, Applicant believes that claims 1-22 are in condition for allowance, and respectfully requests withdrawal of the §103(a) rejections.

Respectfully submitted,



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